HP 64782 Emulators for Motorola 68331/332/333/334/336 Microcontrollers

Product Overview

Hewlett-Packard has the microprocessor development solutions that you need to meet time-to-market and quality goals for Motorola 68331, 68332, 68F333, 68334, and 68336 microprocessor-based designs.

HP 64782 emulators come with zero to 8 Mbytes of emulation memory and a 6833x processor in the emulation pod. They support all of the standard emulation features, such as real-time trace and symbolic debug.

The emulator cards plug into a modular cardcage, which connects to your host via RS-232, RS-422, or LAN. Easy-to-use interfaces are offered on IBM-compatible PCs, Sun SPARCstations, and HP 9000 Series 300/400/700 workstations. Additionally, the cardcage's firmware-resident interface can talk to any ASCII terminal.

Designers are assured of a full line of support with modular emulation tools and software support on a wide range of platforms. Hewlett-Packard has integrated the emulator with code development, debug, emulation, software performance analysis, and software test verification into a comprehensive package that will meet your embedded design requirements. You have the choice of selecting the entire development package or only the parts that you need at a specific time.

For PC-hosted embedded development, a real-time C debugger user interface combines the ease of use of a full Microsoft Windows with HP 64700's transparent, real-time emulation. This allows you to debug embedded C programs at the source level, while your target runs at full speed.

Workstation-hosted embedded development is supported with the X/Motif-based HP Embedded Debug Environment, an integrated suite of tools that span the entire software development process. The environment provides easy-to-use measurement capabilities ranging from real-time, nonintrusive analysis to high-level C and C++ source code debugging. In addition, this environment automatically integrates with the HP SoftBench framework to provide a complete CASE environment for embedded software development.
Features

- 20 MHz*, zero-wait-state, and fast termination cycle operation in target memory
- 20 MHz*, zero-wait-state operation in emulation memory
- Fast termination cycle to 10 MHz in emulation memory
- Supports 3.3 V and 5 V processor versions
- Supports any user-selected configuration of the SIM (or SCIM) registers and processor pins while maintaining full emulation features such as symbolic tracing and overlay memory
- Configuration menu for easy emulator setup
- Processor-specific, on-line help in Motorola format
- Display, modification, and high-level interpreted displays of on-chip peripheral registers
- Processor and emulator configuration is cross checked for inconsistencies and incompatible selections; understandable error and warning messages are given
- Reset mode configuration can be target system or emulator driven; either source is included in configuration cross checking
- Reads processor registers and automatically generates startup code
- Customizable foreground monitor
- Background-style monitor uses BDM mode
- Internal 32.768 kHz crystal or external oscillator clock modes supported
- 36-inch probe cable terminating in an active probe
- Unlimited software execution breakpoints

Emulation bus analyzer

- 80 channels available with trace buffer depths of 1K, 8K, 64K, or 256K
- Postprocessed software-based dequeued trace with symbols and source lines
- Eight events, each consisting of address, status, and data comparators
- Events may be sequenced eight levels deep
- Timing and state counts
- Prestore capability

Emulation memory

- The entire emulation memory is dual-ported, which allows modification and display without processor interruption
- Multiprocessor emulation: synchronous start of up to 32 emulators
- Cross triggering from another emulator, logic analyzer, or oscilloscope
- 256 Kbyte, 512 Kbyte, 1 Mbyte, 1.25 Mbyte, 2 Mbyte, 4 Mbyte, 4.25 Mbyte, 5 Mbyte, and 8 Mbyte memory configurations
- Mapping resolution to 256 bytes

Software support

- Real-time operating system measurement tools
- HP language tool chain includes C compiler, assembler, linker, debugger/simulator, debugger/emulator, and branch validator
- Operates with the real-time, software performance analyzer
- Real-time C debugger for PC-hosted development*
- Support for IEEE-695, HP OMIF, Motorola S record and extended Tek HEX file formats (symbols supported with IEEE-695 and HP OMIF)

*Contact your HP 64000 Field Engineer for the latest configuration information, supported processor speeds, QFP adapter set availability, and software options.
Cardcage

The cardcage is the basis for modular emulators and analyzers. It can be disassembled and reassembled easily for cost-saving reconfiguration to support 8-, 16-, and 32-bit processors.

The cardcage contains a combination RS-232-C/RS-422 serial port with a standard 25-pin serial connector. RS-422 can be programmed to operate at rates up to 460K baud.

Networking

In many embedded designs, it is not possible for each member of a design team to have a target system and an emulator. This makes it essential to have remote access from a networked host. The HP 64700 series emulators offer a LAN connection so that you are able to share a central emulator and target from either a PC or work-station. Not only can team members share a common emulator and data-base, but you also have rapid file transfers at rates of up to six mega-bytes per minute for increased productivity. The cardcage connects to all popular Ethernet 802.3 networks through a 10Base2 ThinLAN BNC connector or a 15-pin AUI (attachment unit interface). TCP/IP protocols, LAN gateways, and ARPA/Berkeley standards are supported.

Emulation bus analysis

Emulation bus analysis provides real-time, nonintrusive analysis along with extensive triggering, tracing, and qualification features. Analysis features offer selective tracing, time tagging, prestore, and a selection of trace depths of 1K, 8K, 64K, or 256K. These comprehensive resources combine to solve both simple and complex problems.

Real-time, nonintrusive analysis is achieved through a dual-bus architecture. This allows traces to be set up and reviewed without breaking processor execution. Selective tracing of microprocessor code flow, without breaking execution, is a major strength of the HP 64700 series emulators and analyzers.

Up to eight hardware breakpoint resources, each consisting of address, data, and status event comparators, can be combined in sequential trace specifications, using “find A, followed by B...” constructs up to eight levels deep.

A range comparator can be applied to address or data events at any one of these levels. The analyzer will trigger on and store all subsequent execution, or store only specified execution information.

Precise time tagging of events helps you identify discrepancies in code execution. Each event is logged into the analyzer with an execution time. Bus cycle, instruction, and module duration can be measured at full processor speeds.

Prestore assists you in pinpointing possible problem areas in your code. Prestore can determine which of several different functions is accessing a variable and is responsible for corrupting it.

For example, a foreground monitor can respond to target system interrupts while in a monitor idle loop.

Extensive breakpoint capabilities allow you to define where to stop the execution of code. Software breakpoints can be set up in the emulator, allowing execution to be halted at an instruction point. Real-time hardware break events increase the flexibility and power of this feature, extending functionality to include stopping at processor address, data, status points, or a combination of all three.

Flexible memory configuration

Memory modules are used for emulation memory. Two slots are available on the active probe, allowing you to plug in the amount of memory you need—up to 8 Mbytes. If you initially order less than the maximum, you can easily expand by adding modules. Modules for 256 Kbytes (HP 64171/2A), 1 Mbyte (HP 64171/2B), and 4 Mbytes (HP 64173A) are available. The entire emulation memory is dual-ported with no timing intrusion, allowing you to display and modify critical program variables without halting the target system.

Robust symbolic support

Symbolic debugging is available when using the PC-hosted real-time C debugger, debugger/emulator, and workstation-hosted software tools. Symbolic debugging clarifies trace list interpretation by allowing you to see program symbols in the trace list. This facilitates quick identification of problems involving the interaction of software and hardware. You also can use symbols in emulation commands and expressions to simplify command entries and user interaction.
Workstation-hosted environment

The HP Embedded Debug Environment is a collection of integrated tools that assist you during software development. These tools include the emulator/analyzer user interface, debugger/emulator, debugger/simulator, advanced cross language system, HP Branch Validator, RTOS measurement tools, and the real-time software performance analyzer.

The emulator/analyzer tool gives you the ability to perform trace analysis, set breakpoints, and establish emulator configuration parameters. In addition, the graphical interface tool is integrated with the embedded debug environment, which coordinates high-level software debugging with low-level microprocessor run control.

The debugger/emulator and debugger/simulator share a common user interface for ease of learning. Both support data types, stack backtrace, and stack-resident local variables. The debugger/emulator also works with your code in real time and allows you to set breakpoints directly without having to switch to the emulator/analyzer.

The advanced cross language system includes HP’s ANSI C compiler, assembler, and linker. These tools are integrated with the HP debug environment to provide a comprehensive array of features and functions that address embedded development needs. For example, the combination of the cross language system and debug environment allows you to display memory and symbolic trace information with overlaid C source. This allows you to view your target code from both a high- and low-level perspective to aid in debugging complex problems.

HP Branch Validator verifies software test effectiveness on complete hardware/software systems. This tool provides an easy-to-use environment for branch analysis that supports rapid iteration of the compile-test-analyze loop. Comprehensive reports, resulting from the branch validator sessions, provide detailed feedback on the execution of test suites.

Real-time operating system measurement tools allow you to transparently trace operating system task flow, service call activity, and measure system performance on running systems. These tools support pSOS+, VRTX32, and user-developed operating systems.

The HP debug environment supports many popular language tools from Microtec Research Inc. and Intermetrics, as well as the HP advanced cross language system of compilers, assemblers, and linkers. The debug environment also operates within the optional HP SoftBench environment, which brings advanced CASE tools and techniques to the realm of embedded software design.

Optional software performance analysis enables you to tune and verify the time-critical aspects of your design. These capabilities are provided at both the C source and assembly language levels. Through automated one-key setup, this system quickly identifies code bottlenecks and gathers statistics and timing information that aid in solving time-critical problems. The software performance analyzer operates with HP 9000 Series 300/400/700 workstations and Sun SPARCstations.

PC-hosted environment

The real-time C debugger (HP B3624A*) is a mouse-driven Microsoft Windows-based, graphical user interface for HP 64700 emulators. The debugger takes full advantage of the emulator’s dual-bus architecture and dual-ported memory to perform many C and assembly debug functions while the target runs at full speed. This means that C debugger functions such as setting breakpoints, display and edit of C variables, and measurement of C program behavior can now often be performed without interrupting program execution. This traditionally could be performed only when a user program was stopped.

Terminal mode operation

A firmware-resident ASCII terminal interface is embedded in the emulator, supplying commands for all emulation and analysis features. Commands are ASCII strings; file transfers using industry-standard formats are accepted. Since a terminal can access these commands, host independence is realized.

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Specifications and Characteristics

Processor compatibility
The HP 64782 emulator supports the Motorola 6833x family microprocessors operating at clock speeds up to 33 MHz.* The emulator supports both 5V and 3.3V operation. The emulator terminates in an AMP socket, and it can be plugged into a PQFP target system using optional accessories.

Environmental

Temperature: operating, 0° to +40°C (+32° to +104°F); nonoperating, -40°C to +70°C (-40°F to +158°F).
Altitude: operating/nonoperating 4600 m (15 000 ft).
Relative humidity: 15% to 95%.

Regulatory compliance
(When installed in HP 64700 cardcage)

Electromagnetic interference:
group 1 class A
3 V/m, 80% modulation,
26 MHz–1000 MHz:
IEC 801-3:1984/EN 50082-1 (1992):
3 V/m, 80% modulation,
26 MHz–1000 MHz
0.5 kV signal lines, 1 kV power lines

Safety: self-certified to UL 1244,
IEC 1010-1, CSA-C22.2 no. 231
Series-M89

Physical

Emulator dimensions: 173 mm
height x 325 mm width x 389 mm
depth (6.8 in. x 12.8 in. x 15.3 in.)
Cable length: emulation control
card to probe, approximately 914 mm
(36 inches).
Probe weight: 0.3 kg (10 oz).
Probe dimensions:

Electrical

Maximum clock speed: 33 MHz*
(with limitations shown in the table):

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Signal</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input High Voltage</td>
<td>V_H</td>
<td>0.7 * V_DD</td>
<td>0.3 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Low Voltage</td>
<td>V_L</td>
<td>V_SS - 0.3</td>
<td>0.2 * V_DD</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Undershoot</td>
<td></td>
<td>-1.0 V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hi-Z (Off-State) Leakage Current @ V_in = GND or V_DD</td>
<td>I_OZ</td>
<td>-20</td>
<td>20 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Signal Low Input Current</td>
<td>RESET</td>
<td>I_L</td>
<td>0.8 mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>All other signals</td>
<td></td>
<td>100 mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Signal High Input Current (V_H = V_DD) All Signals</td>
<td>I_H</td>
<td>50 mA</td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<tr>
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<td></td>
<td>V_OL</td>
<td>4.5 V</td>
<td></td>
<td></td>
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<tr>
<td>Input Capacitance</td>
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<td>C_in</td>
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DC electrical specifications
(V_DD and V_DDSYN = 5.0 Vdc ±10%, VSS = 0 Vdc)

Load Capacitance Drawn from Target System: 250 mA

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AC timing specifications

All specifications are the same as listed in the Motorola MC68323 User's Manual, except for the following.*

\[(V_{DD} \text{ and } V_{DDSYN} = 5.0 \text{ Vdc} \pm 10\%, \ V_{SS} = 0 \text{ Vdc})\]

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<thead>
<tr>
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<tr>
<td></td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
</tr>
<tr>
<td>F1</td>
<td>0.13</td>
<td>16.78</td>
<td>0.13</td>
</tr>
<tr>
<td>1</td>
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<tr>
<td>1A</td>
<td>ECLK Period</td>
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<tr>
<td>1B</td>
<td>External Clock Input Period</td>
<td>59.6</td>
<td>47.7</td>
</tr>
<tr>
<td>2,3</td>
<td>Clock Pulse Width</td>
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<td>16</td>
</tr>
<tr>
<td>2A,3A</td>
<td>ECLK Pulse Width</td>
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<td>183</td>
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<tr>
<td>2B,3B</td>
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<td>29.8</td>
<td>23.8</td>
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<tr>
<td>4,5</td>
<td>Clock Rise and Fall Time</td>
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<td>5C</td>
<td>CLKOUT Buffer Delay</td>
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<td>5</td>
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<tr>
<td>6</td>
<td>Clock High to Address, FC, Size, RMC Valid</td>
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<tr>
<td>6A</td>
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<td>6B</td>
<td>Clock High to Address, FC, Size, RMC Invalid</td>
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</tr>
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</tr>
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<td>10A</td>
<td>Address, FC, Size, RMC Valid to AS, CS Asserted</td>
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<td>27</td>
</tr>
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<td>11A</td>
<td>Address, FC, Size, RMC Invalid to AS, CS (and DS Read)Asserted</td>
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<td>23</td>
</tr>
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<td>12A</td>
<td>Address, FC, Size, RMC Invalid to AS, CS Asserted</td>
<td>-3</td>
<td>27</td>
</tr>
<tr>
<td>13A</td>
<td>AS, CS, DS Negated to Address, FC, Size, RMC Invalid (Address Hold)</td>
<td>-15</td>
<td>10</td>
</tr>
<tr>
<td>14A</td>
<td>AS, CS, DS Negated to Address, FC, Size, RMC Invalid (Address Hold)</td>
<td>-15</td>
<td>10</td>
</tr>
<tr>
<td>14B</td>
<td>AS, CS, DS, CS Read WWidth Asserted (Fast Write Cycle)</td>
<td>100</td>
<td>80</td>
</tr>
<tr>
<td>15A</td>
<td>AS, CS, DS, CS Read WWidth Asserted</td>
<td>45</td>
<td>36</td>
</tr>
<tr>
<td>16A</td>
<td>Clock High to AS, CS, DS, R/W High Impedance</td>
<td>57</td>
<td>45</td>
</tr>
<tr>
<td>17A</td>
<td>Clock High to AS, CS, DS, R/W High Impedance</td>
<td>15</td>
<td>10</td>
</tr>
<tr>
<td>18A</td>
<td>Clock High to R/W High</td>
<td>5</td>
<td>27</td>
</tr>
<tr>
<td>20A</td>
<td>Clock High to R/W Low</td>
<td>5</td>
<td>27</td>
</tr>
<tr>
<td>21A</td>
<td>R/W Asserted to AS, CS Asserted</td>
<td>15</td>
<td>10</td>
</tr>
<tr>
<td>22A</td>
<td>R/W Low to DS, CS Asserted (Write)</td>
<td>70</td>
<td>54</td>
</tr>
<tr>
<td>23A</td>
<td>Clock High to Data Out Valid</td>
<td>27</td>
<td>21</td>
</tr>
<tr>
<td>24A</td>
<td>Data Out Valid to Negating Edge of AS, CS, Fast Write Cycle</td>
<td>15</td>
<td>10</td>
</tr>
<tr>
<td>25A</td>
<td>DS, CS, DS Negated to Data Out Invalid (Data Out Hold)</td>
<td>15</td>
<td>10</td>
</tr>
<tr>
<td>26A</td>
<td>Data Out Valid to DS, CS Asserted (Write)</td>
<td>15</td>
<td>10</td>
</tr>
<tr>
<td>27A</td>
<td>Data In Valid to Clock Low (Data Setup)</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>27B</td>
<td>Late BERR, HALT Asserted to Clock Low (Setup Time)</td>
<td>25</td>
<td>20</td>
</tr>
<tr>
<td>28A</td>
<td>Address, DS Negated to DSACK[10], BERR, HALT, AVEC Negated</td>
<td>0</td>
<td>80</td>
</tr>
<tr>
<td>29A</td>
<td>DS, CS, DS Negated to Data In Invalid (Data In Hold)</td>
<td>0</td>
<td>55</td>
</tr>
<tr>
<td>30A</td>
<td>ClockOUT Low to Data In Invalid (Fast Cycle Hold)</td>
<td>13</td>
<td>8</td>
</tr>
<tr>
<td>31A</td>
<td>ClockOUT Low to Data In High Impedance</td>
<td>-88</td>
<td>70</td>
</tr>
<tr>
<td>33A</td>
<td>DSACK[10] Asserted to Data In Valid</td>
<td>-50</td>
<td>46</td>
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<tr>
<td>35A</td>
<td>BERR Asserted to BERR Asserted (RMC Not Asserted)</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>37A</td>
<td>BGACK Asserted to BG Negated</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>39A</td>
<td>BG Width Negated</td>
<td>2</td>
<td>2</td>
</tr>
<tr>
<td>46A</td>
<td>R/W Asserted (Write or Read)</td>
<td>150</td>
<td>115</td>
</tr>
<tr>
<td>47A</td>
<td>Asynchronous Input Setup Time BR, BGACK, DSACK[10], BERR, AVEC, HALT</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>48A</td>
<td>Asynchronous Input Hold Time</td>
<td>13</td>
<td>10</td>
</tr>
<tr>
<td>49A</td>
<td>Clock High to Data Out High Impedance</td>
<td>55</td>
<td>48</td>
</tr>
<tr>
<td>50A</td>
<td>Clock High to Data Out High Impedance</td>
<td>26</td>
<td>21</td>
</tr>
<tr>
<td>55A</td>
<td>R/W Asserted to Data Bus Impedance Change</td>
<td>40</td>
<td>32</td>
</tr>
<tr>
<td>56A</td>
<td>ClockLow to Data Bus Driven (Reset Instruction)</td>
<td>512</td>
<td>512</td>
</tr>
<tr>
<td>60A</td>
<td>ClockLow to Clock Low (Show)</td>
<td>5</td>
<td>5</td>
</tr>
<tr>
<td>73A</td>
<td>BKPT Input Setup Time</td>
<td>n/a</td>
<td>n/a</td>
</tr>
<tr>
<td>74A</td>
<td>BKPT Input Hold Time</td>
<td>n/a</td>
<td>n/a</td>
</tr>
<tr>
<td>75A</td>
<td>Mode Select Setup Time</td>
<td>20</td>
<td>20</td>
</tr>
<tr>
<td>76A</td>
<td>Mode Select Hold Time</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>77A</td>
<td>RESET Assertion Time</td>
<td>4</td>
<td>4</td>
</tr>
<tr>
<td>78A</td>
<td>RESET Rise Time</td>
<td>10</td>
<td>10</td>
</tr>
</tbody>
</table>

*Contact your HP 64000 Field Engineer for more specific timing specifications for emulators for 68F333 and 68336.
## Terminal-Based Emulation System

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>64782B*</td>
<td>20 MHz active probe emulator for 68331 PQFP processors (includes demo board)</td>
</tr>
<tr>
<td>64782C*</td>
<td>20 MHz active probe emulator for 68332 PQFP processors (includes demo board)</td>
</tr>
<tr>
<td>64782D*</td>
<td>16.78 MHz active probe emulator for 68333 PQFP processors (includes demo board)</td>
</tr>
<tr>
<td>64782E*</td>
<td>20 MHz active probe emulator for 68334G PQFP processors (includes demo board)</td>
</tr>
<tr>
<td>64782G*</td>
<td>16.78 MHz active probe emulator for 68336 PQFP processors (includes demo board)</td>
</tr>
</tbody>
</table>

**Emulation System Options**

<table>
<thead>
<tr>
<th>Model</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>64172A</td>
<td>256 Kbyte, SRAM memory module (20 ns)</td>
</tr>
<tr>
<td>64172B</td>
<td>1 Mbyte, SRAM memory module (20 ns)</td>
</tr>
<tr>
<td>64173A</td>
<td>4 Mbyte, SRAM memory module (25 ns)</td>
</tr>
<tr>
<td>64037A</td>
<td>RS-422 interface card for PC compatibles</td>
</tr>
<tr>
<td>64708A</td>
<td>Software performance analyzer card, (supported on HP 9000 Series workstations, and Sun SPARCstations, HP B1487A software, required)</td>
</tr>
<tr>
<td>64023A</td>
<td>CMB cable (4m long; includes three 9-pin connectors)</td>
</tr>
<tr>
<td>64794A</td>
<td>8K deep 80-channel emulation bus analyzer</td>
</tr>
<tr>
<td>64794C</td>
<td>64K deep 80-channel emulation bus analyzer</td>
</tr>
<tr>
<td>64794D</td>
<td>256K deep 80-channel emulation bus analyzer</td>
</tr>
<tr>
<td>E3407A</td>
<td>AMP socket to 132-pin PQFP/CQFP adapter</td>
</tr>
<tr>
<td>E3433A*</td>
<td>144-pin PQFP adapter</td>
</tr>
<tr>
<td>64171A</td>
<td>256 Kbyte, SRAM memory module (35 ns)</td>
</tr>
<tr>
<td>64171B</td>
<td>1 Mbyte, SRAM memory module (35 ns)</td>
</tr>
</tbody>
</table>

## Software Options for Workstations

For each software model number ordered, purchase one media option and at least one license option for each concurrent user.

- B3092B  Graphical emulator/analyzer
- B1466B  Debugger/simulator
- B1473A  Debugger/emulator
- B1487A  Software performance analyzer (requires HP 64708A analyzer card)
- B1418A  Branch Validator
- B3080A  Real-time operating system measurement tool for pSOS+
- B3081A  Real-time operating system measurement tool for VRTX32
- B3082A  Custom real-time operating system measurement tool

## Advanced Cross Language Tools

- B3640A  Assembler/linker
- B3641A  ANSI C cross compiler

## Media/License Options

- Opt AAH  HP 9000 Series 300/400 manuals/media (DDS DAT tape)
- Opt AAX  HP 9000 Series 300/400 manuals/media (1/4 inch cartridge tape)
- Opt UBX  HP 9000 Series 300/400 single user license
- Opt AAY  HP 9000 Series 700 manuals/media (DDS DAT tape)
- Opt UBY  HP 9000 Series 700 single user license
- Opt AAV  Sun SPARCstation manuals/media (1/4 inch cartridge tape)
- Opt UBK  Sun SPARCstation single user license

## Software Options for PCs

- B3624A*  Real-time C debugger interface

## Advanced Cross Language Tools

- B3640A  Assembler/linker
- B3641A  ANSI C cross compiler

## Media/License Options

- Opt AJ4  IBM 3 1/2" manuals/media
- Opt AJ5  IBM 5 1/4" manuals/media
- Opt UDY  IBM single user license

## Software Support

HP provides software upgrades through the purchase of the software materials subscription (SMS) service. Contact your HP field engineer for more information.

* Contact your HP 64000 Field Engineer for the latest configuration information, supported processor speeds, QFP adapter availability, and software options.
HP Sales and Support Offices

For more information, call your local HP sales office listed in your telephone directory, or an HP regional office listed below for the location of your nearest sales office.

**United States:**
Microprocessor Hotline  
(800) 447 3282

Hewlett-Packard Company  
Test and Measurement Organization  
5301 Stevens Creek Blvd.  
Bldg. 5L-SC  
Santa Clara, CA 95052-8050  
1 800 452 4844

**Canada:**
Hewlett-Packard Canada Ltd.  
5150 Spectrum Way  
Mississauga, Ontario  
L4W 5G1  
(416) 206 4725

**Europe:**
Hewlett-Packard  
European Marketing Centre  
P.O. Box 999  
1180 AZ Amstelveen  
The Netherlands

**Japan:**
Yokogawa-Hewlett-Packard Ltd.  
Measurement Assistance Center  
9-1, Takakura-Cho, Hachiouji-Shi,  
Tokyo 192, Japan  
(81) 426 48 0722

**Latin America:**
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Latin American Region Headquarters  
5200 Blue Lagoon Drive  
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Miami, Florida 33126  
U.S.A.  
(305) 267 4245/4220

**Australia/New Zealand:**
Hewlett-Packard Australia Ltd.  
31-41 Joseph Street  
Blackburn, Victoria 3130  
Australia  
Melbourne Caller 272 2555  
(008) 13 1347

**Asia Pacific:**
Hewlett-Packard Asia Pacific Ltd.  
17-21/F Shell Tower, Time Square,  
1 Matherson Street, Causeway Bay,  
Hong Kong  
(852) 399 7070

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